2102440 Introduction to Microprocessors

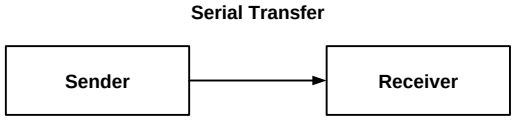
Chapter 12
Serial Communications

Suree Pumrin, Ph.D.

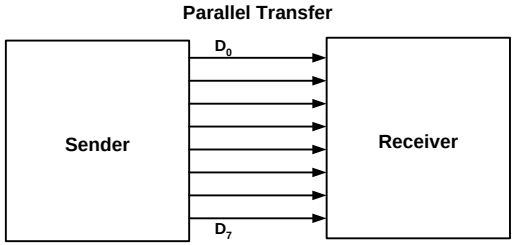
Topics

- Sync vs Asynchronous
- RS-232C
- 8251 USART
- 8251 Initialization

Serial vs. Parallel Data Transfer



Serial communication uses a single line data.

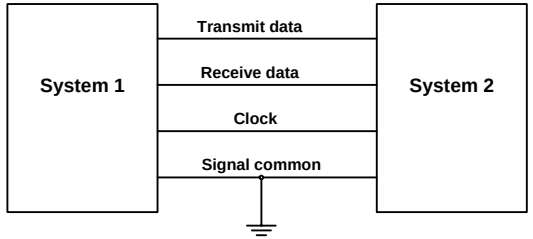


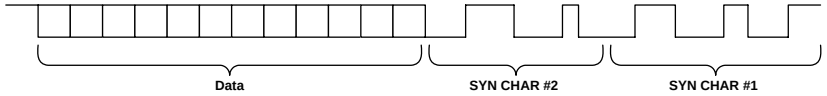
Parallel communication uses n-bit data line.

Synchronous vs. Asynchronous

- A communication protocol is a convention for data transmission that include such functions as timing, control, formatting, and data presentation. There are two categories depending on the clocking of the data on the serial link:
  - Synchronous protocols--each successive datum in a stream of data is governed by a master clock and appears at a specific interval in time.
  - Asynchronous protocols--successive data appear in the data stream at arbitrary times, with no specific clock control governing the relative delays between data.
- There are special IC chips made for serial data communications. These chip is called UART (universal asynchronous receiver-transmitter) and USART (universal synchronous-asynchronous receiver-transmitter).

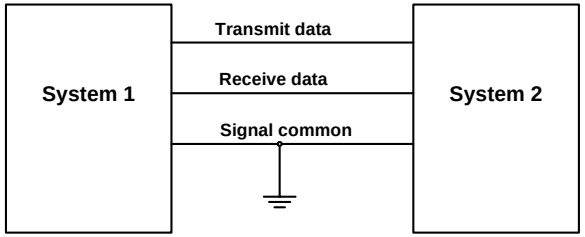
Synchronous Data Communication

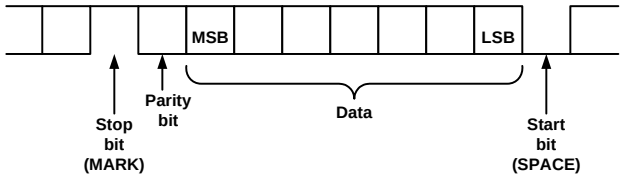




Synchronous data-transmission format

Asynchronous Data Communication



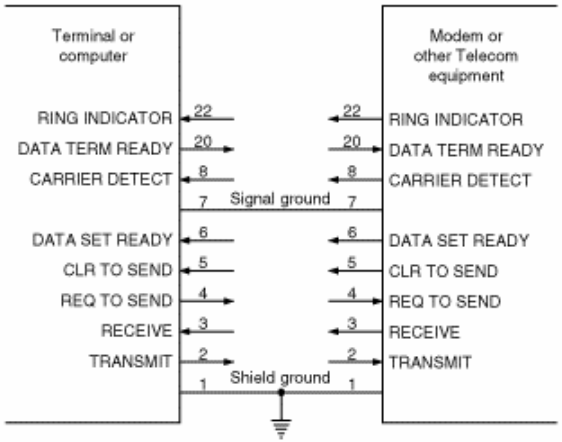


Asynchronous data-transmission format

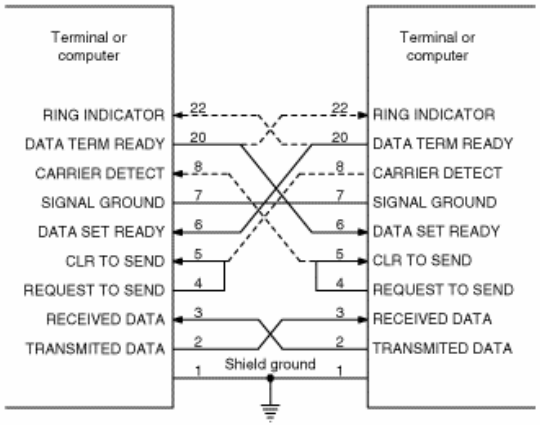
RS-232C

- A widely accepted interface standard originally developed to foster data communication on public telephone network through a modem (modulator-demodulator). This has been adapted to the communication of terminals (PCs) directly to computers.

RS-232C interface with communications equipment



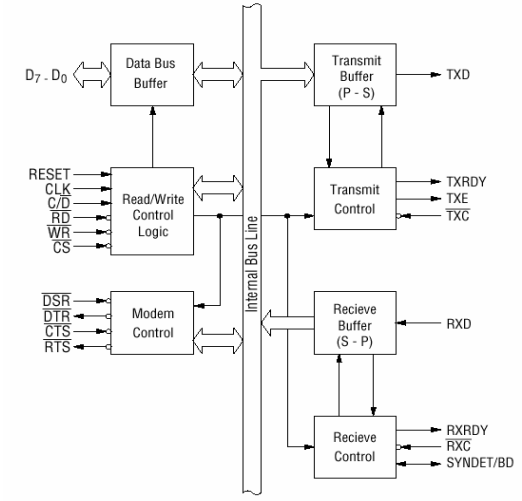
RS-232C Interface, Terminal/computer to Terminal/computer



8251 USART

- The 8251 USART (Universal Synchronous Asynchronous Receiver Transmitter) is capable of implementing either an asynchronous or synchronous serial data communication.
- As a peripheral device of a microcomputer system, the 8251 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

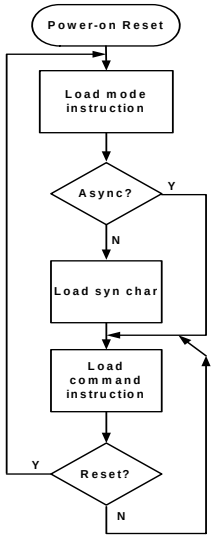
Block diagram of 8251



Read/write operation of 8251

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

8251 Initialization



- Before the 8251 can be used to receiver or transmit characters, its mode control and command registers must be initialized.
- The 8251 has only one address for a few control registers.
- The only readable register is a status register. The other registers must be written in sequence.